Application Note AN100

Electrostatic Discharge Protection for *Open Dots*® Devices

Introduction

Open Dots® powered devices can be subject to electrostatic discharges (ESD) when they are placed on an Open Dots® surface. This is particularly true in dry climates, and more so during the winter months.

If the enablement uses discrete diodes for rectification, ESD protection is often required to prevent diode failure. This application note details two suitable means of ESD protection for robust products.

ESD events present extremely fast voltage and current rise-times to the contacts. What is at issue is that these rise-times can create large voltages across the parasitic inductances of the diode packages. As a result, large voltages can be present back-biasing a diode to the point of breakdown failure before the partner diode begins to conduct enough to protect it.

A capacitor can be used to slow the rise-times such that the parasitic inductances cannot generate voltage drops beyond the diode ratings. Care must be taken to minimize package inductances and other sources of high-frequency impedances.

Below are some schemes that can be used to slow down the ESD rise-times such that each diode of a diode pair can suitably protect its partner.

Power and Ground Plane Approach Schematic

In this approach, a multilayer printed circuit board, for example, a four layer board, is used to provide a continuous ground plane and a continuous power plane over a substantial portion of the *Open Dots*® receiver. The two remaining layers can be used for routing the remainder of the circuit as required. The ground plane connects to the anodes of the lower diodes, and the power plane connects to the cathodes of the upper diodes.

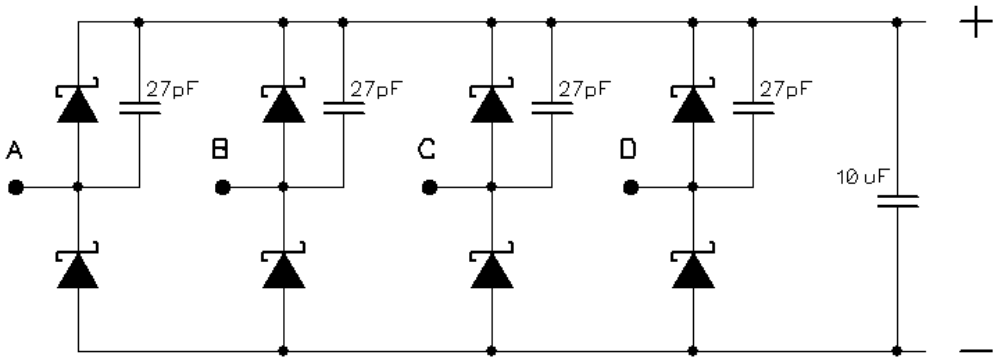

Figure 1: Power and Ground Plane ESD Protection Schematic

This is an excellent approach, because the power and ground planes provide a very stable, low-impedance path to the supply rails even at very high frequencies. This is suitable for reducing the overall lead inductance of the conducting diode so that the reverse biased diode remains protected. As a side-benefit, the planes will also reduce undesired EMI emissions from the rest of the circuit, such as from switching regulators, which are notorious for their unexpected emissions.

Power and Ground Approach Layout

The layout should incorporate very short traces for the diode junctions, very short traces for the bypass capacitors, and very short traces from the diodes to the power and ground planes.

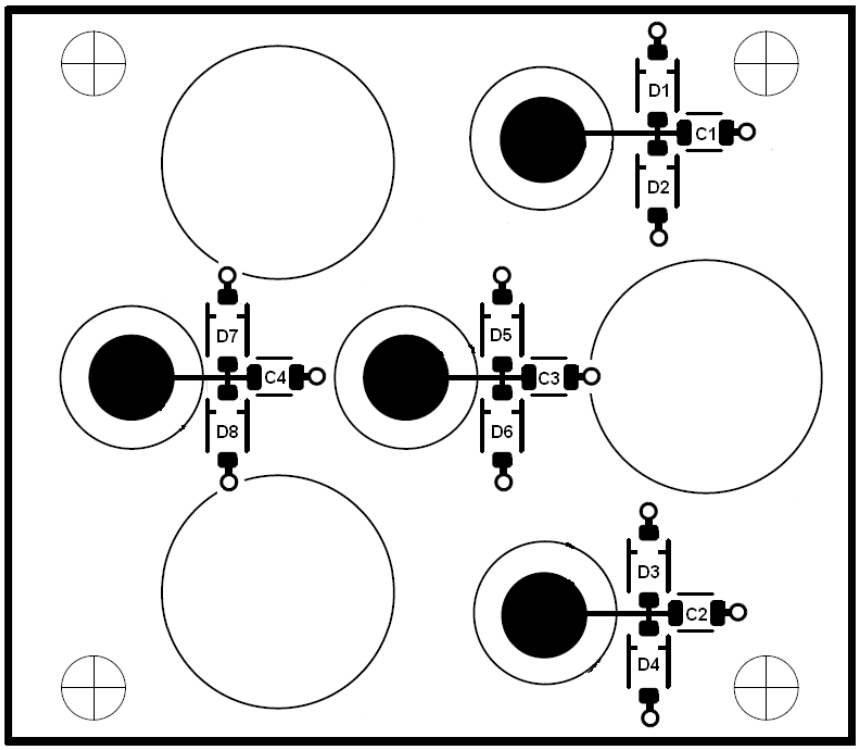

Figure 2: Power and Ground Plane ESD Protection Layout

The critical area for proper protection is the single point at which the two diodes and single capacitor intersect. What is not important is the trace length from the contact to the point of intersection. There are other ways to lay out the components to achieve the same ESD protection, so long as the trace lengths from each component to the intersection point is kept short, and the vias to power and ground are held close to the components.

Please note that for a power or ground plane to remain effective, they must be uninterrupted for the most part. Therefore avoid routing on these layers, because this will necessarily introduce non-conductive keep-out gaps that reduce the effectiveness of the planes. Small keep-outs, such as for vias, are rarely found to degrade the properties of planes.

Bypass Capacitor Approach Schematic

We now turn to another approach helpful for cases when a multi-layer board is not present or otherwise impractical. In this case, ESD protection is achieved by filtering the contact net using three capacitors forming a Y network. In this scheme the Y network provides a uniform, low-inductance virtual ground regardless of the polarity of the ESD voltage.

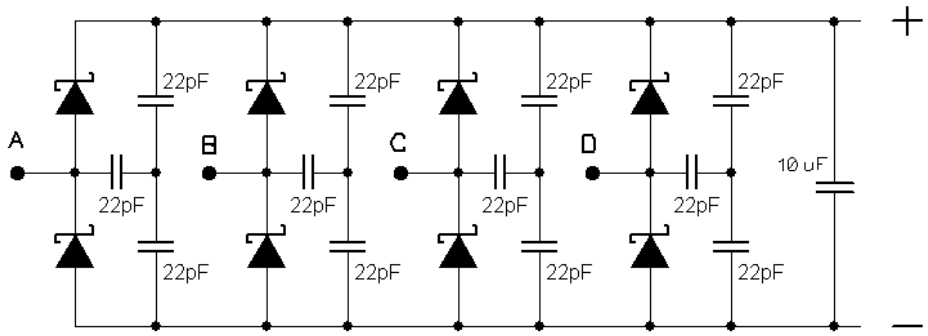

Figure 3: Bypass Capacitor ESD Protection Schematic

Using Bypass Capacitor Approach Layout

Again, the dominant issue is that the traces must be made to be very short in order to achieve adequate protection. The layout should incorporate very short traces for the diode junctions, very short traces for the bypass capacitors, and very short traces from the diodes to the power and ground planes. Of less importance is the length of the trace from each contact point to its respective rectification input node.

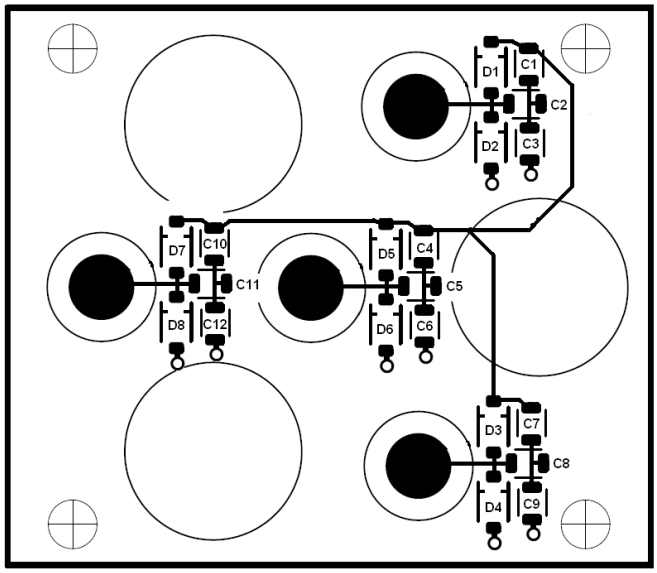

Figure 4: Bypass Capacitor ESD Protection Layout

In fact, the diodes could all be located in a single corner of the printed circuit board, with traces to the contact points meandering around the periphery of the board so as not to interfere with other circuits.

Conclusion

Various methods of preventing damage to a rectifier when its inputs are exposed to aggressive ESD events are described. It is believed that events with very high dI/dt produce large voltages across package inductances, destroying the reverse biased diode of a given pair.

By adding capacitance to the input nodes, the magnitude of dI/dt is reduced to the point where the lead inductances no longer produce voltages in excess of the diode ratings. To apply this effectively, care must be taken at every step to ensure that package inductances do not dominate the reactive impedance.

Two methods are described herein that provide adequate protection from ESD events.